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PROCESS VARIATION INDUCED MISMATCH ANALYSIS IN SENSE AMPLIFIERS

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ABSTRACT

A Sense Amplifier is a very critical peripheral circuit in the memories as its performance strongly affects both the memory access time and the overall memory power dissipation. As the device dimensions scale below 100 nm, the process variations are increasing and are impacting the circuit design significantly. In this research paper, the effects of process variation induced transistor mismatch on the sense amplifier performance are studied. A comparative study of the effect of mismatch on the delay for different sense amplifier configurations at 45 nm technology is presented.

Keywords: Process Variation, Mismatch Analysis, Sense Amplifiers, SRAM, Voltage Mode Sense Amplifier, CMOS.

INTRODUCTION

The process of technology scaling has enabled us to integrate large memory blocks with logic circuits on a single chip. However, the performance of the on-chip memory limits the speed and the performance of the overall system. The key limiting factor is the increasing bit line capacitance, which results in the increased efficient memory designs, both this time and the signal swing on the bit lines need to be minimized [1, 2]. A sense amplifier is used to generate full rail output voltage by using minimum bit line differential voltage/current. As CMOS IC fabrication technology becomes more and more advanced, the control of process variation and manufacturing uncertainty becomes more and more critical [2-5]. The sense amplifier performance degradation due to the process variations and the resulting yield loss is more pronounced than before. It is important for the designer to be able to understand mismatch effects, since the sensing should be done as fast as possible, subject to the sensitivity constraints imposed by the parameter variations inherent in the fabrication process [4, 5]. For low power applications, it is always desirable to have a low bit line differential voltage. However, the bit line differential voltage has a direct impact on the yield of the sense amplifier [1, 3].This research paper studies the effect of the length mismatch and the threshold voltage mismatch on the sense amplifier designs at 45 nm CMOS technology. The variations in the sensing delay with the transistor mismatch are compared in voltage mode and the current mode sense amplifier. Section 2 gives a brief introduction to the process variations. Section 3 briefly describes the sense amplifiers to be used in this study. Section 4 explains the experimental set-up for mismatch analysis. Section 5 documents the simulation results and the conclusions are presented in Section 6.

Process Variations in SA

The inter-die and the intra-die variation in the process parameters (channel length (L), width (W) and transistor threshold voltage (V_t) in nanoscale technologies can significantly degrade the yield of an SRAM design. If V_t is the variation in between the sense transistors is sufficient to overcome the bit differential voltage developed on the bit lines of the SA, then the SA may latch incorrect signal. Thus, the V_t variation in the transistors in the SRAM cell causes the read, write, access and hold failures in the cell [2, 4]. On the other hand, the statistical variations in the device parameters also result in the significant variation in the sensing delay (the difference between the time sense amplifier is turned "ON" and the time sense amplifier outputs are available) of the sense amplifier used in SRAM's and in the worst case may amplify the input signal in the wrong direction

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(functional failure due to incorrect sensing). The access failure in SRAM is defined as the reading of the wrong data during the access of the memory array. The access failure in an SRAM array can occur due to the random V_t variation in the SRAM cell or sense amplifier. Hence, the analysis of access failure has to consider the impact of both the SRAM cell and sense amplifiers [1, 3].

Sense Amplifiers

This section briefly illustrates the working of the sense amplifiers to be used in this study:

Voltage Mode Sense Amplifier (VSA)

A Sense Amplifier implicates the whole memory and is required to have a high performance and high yield which is actually determined by its robustness. The performance is determined primarily by the sensing delay [3, 4]. The robustness is determined by the minimum voltage difference the two bit lines that can be correctly sensed (input offset voltage). Thus, the principal design goal in CMOS sense amplifier design is to lower the sensing delay and to reduce the input offset voltage at which the sensing is done [2, 4]. In Figure 1, we show the design of a basic voltage mode.

The current flow of the differential input transistors N1 and N2 controls the serially connected latch circuit. A small difference between the currents through N1 and N2 converts to a large output voltage. A drawback of a latch type sense amplifier is that once the decision process has started, the positive feedback cannot be recovered without resetting the circuit to a meta stable point [1, 3].

Current Mode Sense Amplifier (CSA)

The current sense amplifier consists of two parts: current conveyor circuit with unity-gain current transfer characteristics and the second is the current sense amplifier that senses the differential current as shown in Figure 2. The current conveyor circuit consists of four equally sized PMOS transistors (P1 to P4) with positive feedback. The intermediate nodes are pre-equalized by using a PMOS in order to prevent the latching and to ensure the same delay for all read cycles [1, 3, 4]. The current conveyor circuit output is connected to the second current sense amplifier. All the nodes of the circuit has been pre-charged to full V_{DD} or pre-discharged to ground. The operation of the circuit is in two phases. In pre charge phase, the bit lines and the output nodes of S_A and S_B are pre-charged high. This causes the nodes A and B to be pre-discharged to ground [3, 4, 5]. In the evaluation phase, Y_{sel} is grounded and the current is immediately transported to the nodes A and B through the drain of P3 and P4. The difference in the current flowing through A and B will be equal to the cell current. The sense amplifier is enabled to the two inverter delay after the SA_{en} is pulled high during which the bias current flows through the two legs of the sense amplifier while the PMOS (M) keeps the output equalized [3, 4]. After this two inverter's delay, the PMOS (M) is disabled and the differential current flowing through the sense amplifier causes a differential voltage to be developed at SA and SA#. This differential voltage is then amplified to the CMOS logic levels by the high gain positive feedback cross-coupled inverters [1, 3]. The sensing delay is relatively insensitive to the bit line capacitance, as this technique does not depend on the differential discharging of the large bit line capacitances [3, 4].

Experimental Set-Up

The sense amplifier is aid to be perfectly balanced or symmetric when all the transistor parameters on the left hand side are equal to the parameters on the right hand side. It is said to be vertically matched when the W/L's of the NMOS and the PMOS have been ratioed so that the sense amplifier has equal pull-up and pull-down capability. For mismatch analysis, we consider only the variation in the channel length and the threshold voltage of the transistors [2, 3]. Our analysis assumes that a particular parameter x (where x is neither L, W or V_{th} of the device), is varied by decreasing the value of that parameter for the NMOS transistors in the left hand side of the sense amplifier by Δx and increasing it by the same amount for corresponding right hand side transistors. We assume perfect matching in the PMOS transistors while performing the mismatch analysis of the NMOS transistors and vice-versa. In all sense amplifiers, the total width of all the transistors is kept nearly the same for fair comparison. The simulations are carried out for 45 nm CMOS technology by using the Predictive Technology Model (PTM) [1, 4, 5]**.**

Simulation Results

Extensive simulations are carried out in order to check the effect of mismatch in V_{th} and the channel length.

Mismatch in NMOS Parameters

For the circuit shown in Figure 2, V_{th} of M1 is decreased and that of M3 is increased by the same amount. For the circuits shown in Figure 1, the V_{th} of N1 and N3 is decreased while that of N2 and N4 is increased. Similar analysis is carried out to study the channel length mismatch in the NMOS transistors. For all the simulations, we assume that the SRAM cell content is logic high, since this gives the worst case results for the above set-up [2, 3]. The results of the delay versus the NMOS threshold voltage mismatch are shown in Figure 4. However, the CSA is relatively more sensitive to mismatch in the NMOS threshold voltage which fails at 2%. Similar trend is observed with the NMOS length mismatch. However, if the minimum length (i.e 50 nm) NMOS transistors are used, the CSA is found to become

extremely sensitive to mismatch in the channel length [2, 4, 5]. The simulation results for the NMOS length mismatch are shown in Figure 3.

From Figure 3, we find that the sensing delay increases with the mismatch. However, the delay decreases when a logic low is read with the same set up. Exactly, the reverse phenomenon can be expected, if the parameters of the NMOS transistors in the left hand side are increased while those in the right hand side are decreased [1, 3, 4].

Mismatch Analysis in PMOS Parameters

The parameter mismatch of the PMOS transistors does not drastically affect the performance of the sense amplifier. The reason being, when the sense amplifier is activated the NMSO transistors immediately start operating in the saturation region, however the PMOS transistors operate either in the cut-off or conduct in the deep triode region [4, 5]. The mismatch analysis is carried out by decreasing the V_{th} of M2 and increasing the V_{th} of M4 by the same amount. Similar variations in the channel length are imposed in order to understand the effect of the length mismatch. The readings are taken when the SRAM cell content is logic low, as this gives the worst case results [1, 3, 4].The simulation results for length mismatch and the threshold voltage mismatch are shown in Figure 5 and Figure 6 respectively. However, the sense amplifier delay decreases when the logic high is read from the memory. The simulation results show that the VSA is less sensitive to the variations in the PMOS parameters.

Fig 1. Voltage Mode Sense Amplifier (VMSA)

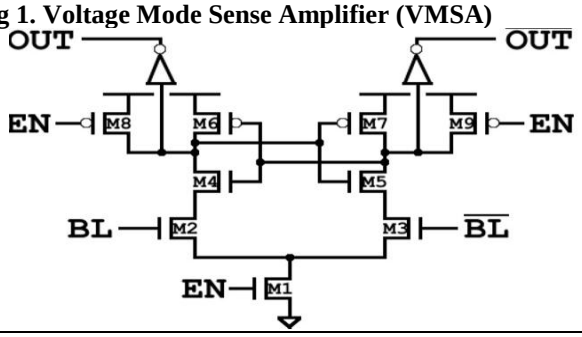


Fig 2. Current Mode Sense Amplifier (CMSA)

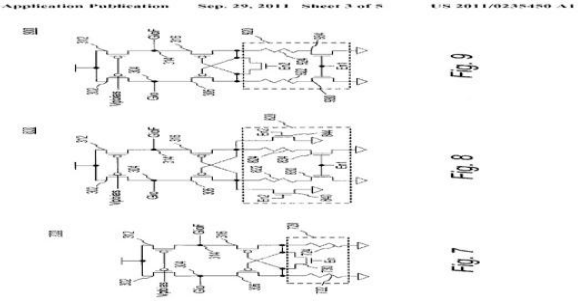


Fig 3. Sense Amplifier Delay versus NMOS Channel Length Mismatch

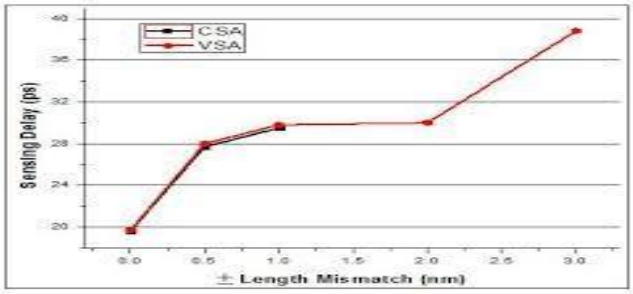


Fig 4. Sense Amplifier Delay versus NMOS Threshold Voltage Mismatch

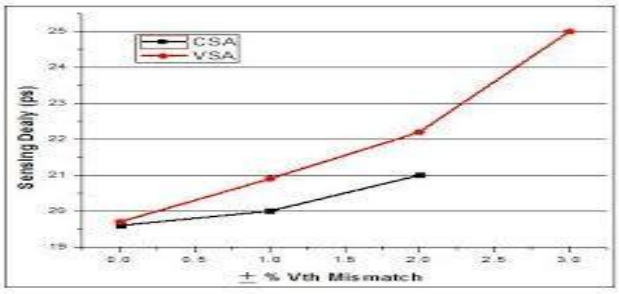


Fig 5. Sense Amplifier Delay versus PMOS Channel Length Mismatch

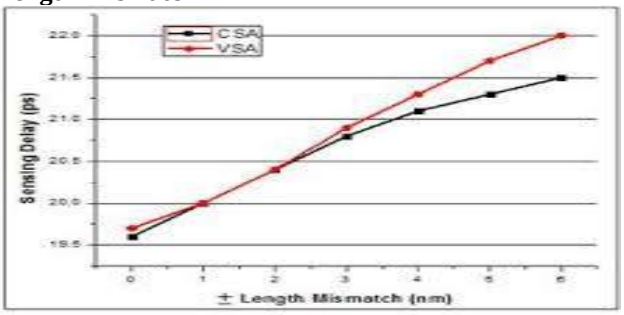
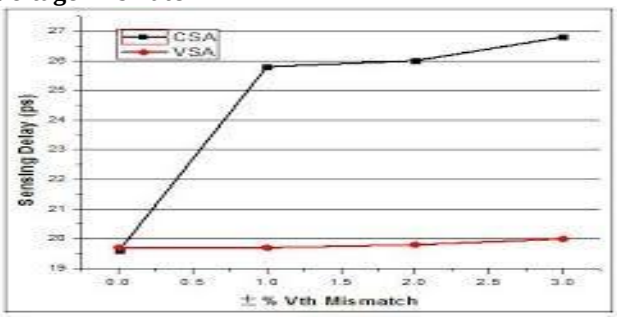


Fig 6. Sense Amplifier Delay versus PMOS Threshold Voltage Mismatch



CONCLUSION

The impact of process variation induced transistor mismatch on two different sense amplifier configurations is presented. It is found that as the mismatch increases the sensing delay also increases, eventually leading to the failure of the sense amplifier. The performance of the sense amplifier is worst affected by the mismatch in NMOS transistor threshold voltage and the channel length whereas the performance degradation due to the PMOS parameter variations is found to be marginal. The current sense

amplifier is found to give the beast performance in terms of speed, although when compared to the voltage sense amplifiers it is marginally more sensitive to the parameter variations.

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CONFLICT OF INTEREST:
The authors declare that they have no conflict of interest.

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